

ATEVK-900-ANT-FM PCB Specification

Table of Contents

1	GENERAL INFORMATION.....	3
1.1	Board identification.....	3
1.2	Contact persons for PCB issues.	3
2	PCB SPECIFICATION	3
2.1	Manufacturing data	3
2.2	Layer stackup	4
2.3	Gerber files.....	5
2.4	Special via considerations.....	5
2.5	Impedance controlled track.....	5
2.6	Placement of fabrication ID mark	5
3	PANELIZING.....	5
4	QUALITY OF SILKSCREEN LAYERS	6

1 General information

1.1 Board identification

Name: ATEVK-900-ANT-FM
Board identification number: A08-2099 Rev1

1.2 Contact persons for PCB issues.

- PCB Designer: sanjay.yadav@atmel.com

2 PCB specification

2.1 Manufacturing data

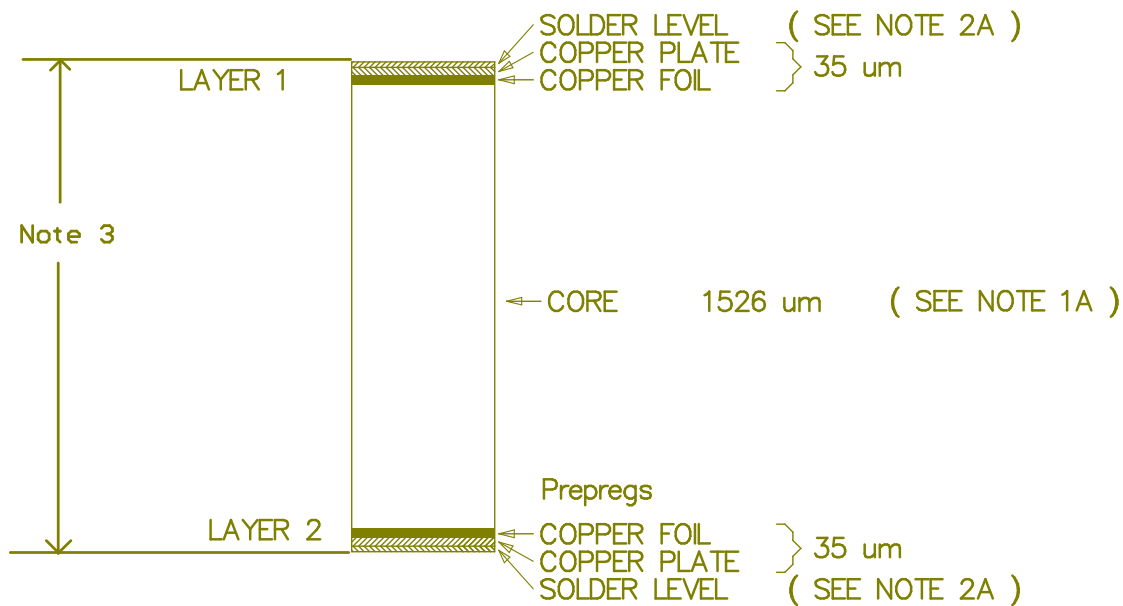
- Size: 23.3mm x 33.3mm
- PCB material: FR-4, 1.6mm thickness
- Layers: 2
- Finish: ENIG
- Minimum via hole size: 0.4mm
- Minimum via pad size: 0.8mm
- Minimum track width: 1.5mm
- Minimum spacing: 0.4mm
- Solder mask color: Black
- Silk-screen color: White

2.2 Layer stackup

Figure 2-1 shows the detailed layer stackup for this PCB.

Figure 2-1 Detailed layer stackup

Layer stackup



NOTE 1A: FR4

2A: SURFACE PROTECTION: Chemical Gold

3: PCB Thickness to be calculated based on Stack up
THE BOARD MUST BE RoHS COMPLIANT

DETAIL A (CROSS-SECTION)

SCALE = NONE

2.3 Gerber files

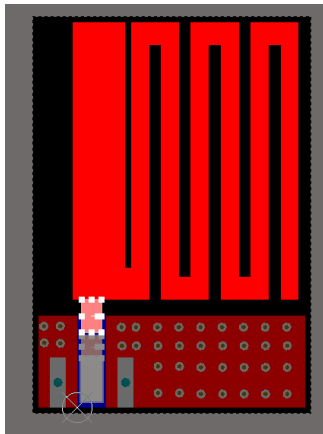
Table 2-1 Layer stackup corresponding Gerber files (listed from top to bottom)

File name	Description
ATEVK-900-ANT-FM_REV1.GTP	Gerber file for top paste-mask
ATEVK-900-ANT-FM_REV1.GTO	Gerber file for top overlay (silkscreen)
ATEVK-900-ANT-FM_REV1.GTS	Gerber file for top solder-mask
ATEVK-900-ANT-FM_REV1.GTL	Gerber file for top layer
ATEVK-900-ANT-FM_REV1.GBL	Gerber file for bottom signal layer
ATEVK-900-ANT-FM_REV1.GBS	Gerber file for bottom solder-mask
ATEVK-900-ANT-FM_REV1.GBO	Gerber file for bottom overlay (silkscreen)
ATEVK-900-ANT-FM_REV1.GBP	Gerber file for bottom paste-mask
ATEVK-900-ANT-FM_REV1.GM1	Gerber file for mechanical 1 layer (board outline)
ATEVK-900-ANT-FM_REV1.DRR	Drill file report
ATEVK-900-ANT-FM_REV1.TXT	Drill file

2.4 Special via considerations

All vias are covered with solder mask on the top and bottom side of the board.

2.5 Impedance controlled track



Selected track should be 50ohm at 1GHz

2.6 Placement of fabrication ID mark

The fabrication ID mark should be placed on the bottom side.

3 Panelizing

When making panels for this board the following issues should be considered.

- Fiducial marks should be placed on the panel.

4 Quality of silkscreen layers

The silkscreen layers for the PCB must be of high quality for several reasons:

- Very small text is used
- Text is close to pads and therefore the mask must be centered properly on the board
- The PCB is used for development boards and therefore the silkscreen is an essential part of the overall product quality.